What is claimed is:

1. A method for removing a silicon carbide layer during fabrication of an integrated circuit chip on a semiconductor wafer comprising:

flowing an etch chemical into proximity with a surface of the semiconductor wafer having the silicon carbide layer and a low dielectric constant material exposed thereon, the etch chemical selected from the group consisting of carbon-tetrafluorite (CF4), trifluoromethane (CHF3), difluoro-methane (CH2F2) and methane (CH4);

introducing a selectivity enhancing chemical into the flow of the etch chemical, the selectivity enhancing chemical increasing the selectivity of the etch chemical to the silicon carbide layer relative to the low dielectric constant material and being selected from the group consisting of hydrogen (H2) and ammonia (NH3); and

etching the exposed silicon carbide layer from the surface of the semiconductor wafer substantially without removing the exposed low dielectric constant material.

2. A method as defined in claim 1 further comprising:

introducing the selectivity enhancing chemical in a C:H:F ratio of about 1:1:2 to about 1:8:4.

3. A method as defined in claim 1 further comprising:

introducing the selectivity enhancing chemical into the flow of the etch chemical prior to flowing the etch chemical into proximity with the surface of the semiconductor wafer.

4. A method as defined in claim 1 further comprising:

introducing the selectivity enhancing chemical into the flow of the etch chemical substantially simultaneously with the flowing of the etch chemical into proximity with the surface of the semiconductor wafer.

5. A method as defined in claim 1 further comprising:

flowing the etch chemical into proximity with the surface of the semiconductor wafer at a temperature in a range of about -30° C to about 80° C, a

pressure in a range of about 5 mT to about 300 mT and a power level in a range of about 200 Watts to about 1500 Watts.

6. A method for performing a damascene metallization process during fabrication of an integrated circuit chip on a semiconductor wafer comprising:

forming a silicon carbide layer on the semiconductor wafer;

forming a layer of a low dielectric constant material on the semiconductor wafer;

removing a region of the low dielectric constant material to expose a portion of the silicon carbide layer and a portion of the low dielectric constant material;

flowing an etch chemical into proximity with the exposed portions of the silicon carbide layer and the low dielectric material, the etch chemical selected from the group consisting of carbon-tetrafluorite (CF4), trifluoromethane (CHF3), difluoro-methane (CH2F2) and methane (CH4);

introducing a selectivity enhancing chemical into the flow of the etch chemical, the selectivity enhancing chemical increasing the selectivity of the etch chemical to the silicon carbide layer relative to the low dielectric constant material and being selected from the group consisting of hydrogen (H2) and ammonia (NH3);

removing a region of the exposed silicon carbide layer with the combined etch chemical and the selectivity enhancing chemical substantially without eroding the exposed portion of the low dielectric constant material; and

forming a metal region into the removed regions of the low dielectric constant material and the silicon carbide layer.

7. A method as defined in claim 6 further comprising:

forming the metal region by depositing copper (Cu) into the removed regions of the low dielectric constant material and the silicon carbide layer.

8. A method as defined in claim 6 further comprising:

introducing the selectivity enhancing chemical in a C:H:F ratio of about 1:1:2 to about 1:8:4.

9. A method as defined in claim 6 further comprising:

introducing the selectivity enhancing chemical into the flow of the etch chemical prior to flowing the etch chemical into proximity with the exposed portions of the silicon carbide layer and the low dielectric constant material.

10. A method as defined in claim 6 further comprising:

introducing the selectivity enhancing chemical into the flow of the etch chemical substantially simultaneously with the flowing of the etch chemical into proximity with the exposed portions of the silicon carbide layer and the low dielectric constant material.

11. A method as defined in claim 6 further comprising:

flowing the etch chemical into proximity with the exposed portions of the silicon carbide layer and the low dielectric material at a temperature in a range of about -30° C to about 80° C, a pressure in a range of about 5 mT to about 300 mT and a power level in a range of about 200 Watts to about 1500 Watts.